RSFQ Circuitry Using Intrinsic π-Phase Shifts

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***Abstract*—The latching of temporary data is essential in the Rapid Single Flux Quantum (RSFQ) electronics family. Its pulse-driven nature requires two or more stable states in almost all cells. Storage loops must be designed to have exactly two stable states for binary data representation. In conventional RSFQ such loops are constructed to have two stable states, e.g. by using asymmetric bias currents. This bistability naturally occurs when phase-shifting elements are included in the circuitry, such as π-Josephson junctions or a π-phase shift associated with an unconventional (d-wave) order parameter symmetry. Both approaches can be treated completely analogously, giving the same results. We have demonstrated for the first time the correct operation of a logic circuit, a toggle-flip-flop, using rings with an intrinsic π-phase shift (π-rings) based on hybrid high-T_c to low-T_c Josephson junctions. Because of their natural bistability these π-rings improve the device symmetry, enhance operation margins and alleviate the need for bias current lines.**

***Index Terms*—Superconducting devices, π-phase shift.**

I. Introduction

RAPID SINGLE flux quantum (RSFQ) electronics is based on connected superconducting rings containing standard Josephson tunnel junctions and bias current sources [1]. Josephson junctions act as gates between superconducting loops for controlled transfer and storage of data, which is represented by magnetic flux quanta $\Phi_0 = h/2e$. This first application of macroscopic quantum effects in digital computing is one of today's most promising candidates to overcome several serious problems in the established CMOS technology [2].

The typical current-voltage characteristic of circuit elements in CMOS technology is replaced by the current-phase characteristic of two terminal devices in superconductor electronics. In this way, the phase difference φ of the macroscopic wave function between the nodes of the circuit elements acts as a new state variable, replacing the voltage.

The operation of RSFQ circuits is based on elementary building blocks for transport, decision, and storage of data [3]. Since RSFQ is a pulse based logic, the temporary latching of data is an essential task in many RSFQ logic cells. Hence, internal states need to be implemented in those cells, which is achieved by using the flux quantization in a superconducting ring structure. The rings have to be designed in such a way as to have exactly two stable states in order to represent binary data.

In comparison to standard junctions, π-junctions exhibit a phase shift of π in their current-phase characteristic. If a π-junction, or a π-phase shift associated with an unconventional order parameter symmetry [4] is included in a superconducting loop, with dimensions of practical interest, a spontaneous circulating current arises to create a second π-phase drop around the loop. Depending on the direction of this current, the second π-phase drop either adds to or subtracts from the initial phase drop resulting in a total phase change around the loop of 2π or 0, respectively. The magnetic flux associated with this persistent circulating current is a fraction of a flux quantum, growing asymptotically to a half flux quantum in the large inductance limit [5]. For convenience we will refer to this spontaneously generated flux as a half flux quantum. These spontaneously generated half flux quanta are the base for building a bistable system in which the polarity of the flux is controllably toggled by passing a current pulse [6]. Such rings can be straightforwardly used for all kinds of cells with internal states. In addition, it has been proposed to use π-junctions in a non-switching mode to reduce the inductance in RSFQ circuits [7] and to employ the self-biasing effect in π-loops for the reduction of bias currents [8]. In this work, instead of π-junctions [9] we use the π-phase shift based on d-wave order parameter symmetry in high-T_c cuprate superconductors.

Here we provide a further description on the first successful integration of π phase-biased superconducting rings in a logic circuit, as reported recently in [10]. A toggle-flip-flop (TFF) was realized whose internal states, represented by the polarity of half flux quanta in π-rings, can be controllably toggled by applying single flux quantum pulses. First we will discuss the stability of storage loops and the advantages of incorporating π-phase shifts in bistable cells. This is followed by a numerical circuit analysis of the TFF, clearly confirming the improved stability due to the incorporation of π-phase shift elements. In the final section we present the practical realization of the device and the experiments demonstrating the controlled toggling of the internal state.

II. Stability of a Storage Loop

To convey the benefits of incorporating intrinsic π-phase shifts in bistable cells, we start by analyzing a storage loop with two junctions as shown in Fig. 1(a). We do not consider connections to other cells for the moment or any currents flowing through the input and output terminals.

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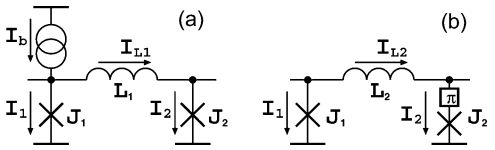

Fig. 1. (a) Conventional storage loop with asymmetric bias current; (b) storage loop with an integrated π-phase shift.

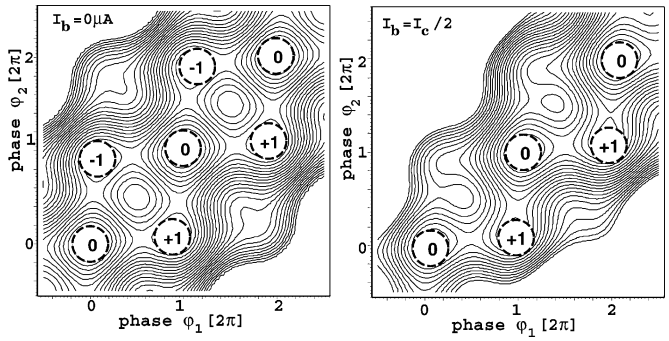

Fig. 2. Contour plot of the free energy for a storage loop with symmetric parameters (a) and with an asymmetric external current source I_b (b). The stable states are marked with the corresponding amount of flux quanta ($\mathbf{A}$: -1, $\mathbf{B}$: 0 or $\mathbf{C}$: $+1$) stored in the loop inductance L_1. In both plots we have used $\beta_L = 2\pi$.

A simple storage loop with two equal junctions J_1, J_2 with critical current I_c according to Fig. 1(a) can be described with the free energy:

$$U(\varphi_1,\varphi_2) = \frac{\Phi_0 I_c}{2\pi}\times \left(2-\cos(\varphi_1)-\cos(\varphi_2)-\varphi_1\frac{I_b}{I_c}\right) + \frac{\Phi_0^2}{8\pi^2}\frac{(\varphi_1-\varphi_2)^2}{L} \quad (1)$$

where φ_1, φ_2 are the phase differences across the junctions, I_b is the asymmetric bias current, and L is the total inductance of the storage loop. The resulting energy landscape from (1) is depicted in Fig. 2 for different values of the bias current. The screening parameter $\beta_L = 2\pi L I_c/\Phi_0$ of the storage loop was chosen to be 2π. The minima in the contour plots correspond to energetically stable states and are marked by the number of flux quanta stored in the loop. Without an external bias current I_b the device is symmetric and the free energy has one, three or a larger odd number of stable states, depending on the loop inductance (see Fig. 2(a)). When the bias current is increased to $I_c/2$, the storage loop becomes bistable as can be seen in Fig. 2(b).

We can plot the free energy as a function of the flux through the loop with the asymmetric current I_b as a parameter and observe its influence on the stability of the states. The plot in Fig. 3(a) shows for normalized bias current $i = I_b/I_c$ the stability of all three states (interpreted as local minima) and the height of the separating barrier (see Fig. 3(b)). When the asymmetric bias current is increased, the state $\mathbf{A}$ vanishes and state $\mathbf{C}$ becomes more stable. For $i \approx 0.5$ the states $\mathbf{B}$ and $\mathbf{C}$ have

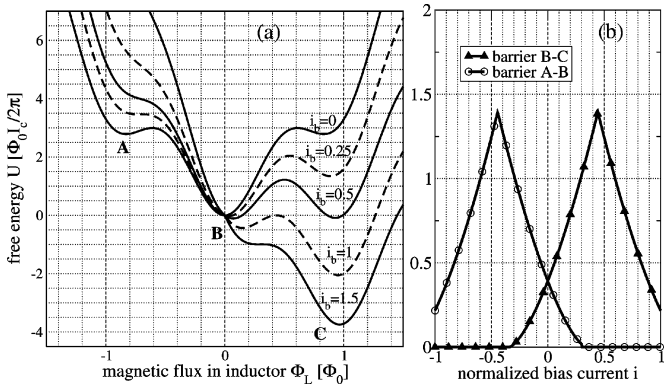

Fig. 3. (a) The free energy versus the magnetic flux $\Phi_L = (\Phi_0/2\pi L)(\varphi_1 - \varphi_2)$ in the inductor L ($\beta_L = 2\pi$) with stable points $\mathbf{A}$, $\mathbf{B}$ and $\mathbf{C}$ for different values of the bias current I_b; (b) the height of the separating barrier between the stable points.

equal free energy and their separating barrier reaches a maximum. This is the ideal configuration for a well designed bistable storage loop in an RSFQ circuit.

A further increase of i results finally in the vanishing of state $\mathbf{B}$ and the system is no longer bistable (see last curve for $i = 1.5$ in Fig. 3(a)). The artificial generation of a two level system makes the design of RSFQ logic cells strongly asymmetric and acts often as the most critical parameter for the correct operation.

In comparison to classical RSFQ circuits with asymmetric configurations, the superconducting loop with an internal π-phase shift (schematic shown in Fig. 1(b)) is an inherent two state system even for low inductance values. In comparison to standard RSFQ circuits, this storage loop is a new circuit element and shows almost the same behavior as the asymmetrically biased loop (see Fig. 4), but it is less sensitive to parameter deviations (as will be shown later) and it does not need any current source—simply due to its topology.

When using asymmetric bias sources, we can not avoid the redistribution currents into other parts of the circuit. These currents complicate the design by requiring a careful optimization of the affected elements in the circuit. With π-loops this effect is strongly diminished, presenting an advantage in RSFQ design.

III. Design and Analysis of Digital Circuits

Due to the enhanced circuit symmetry and reduced need for bias currents, storage loops containing intrinsic π-phase shifts are expected to result in an improved robustness against parameter spread. By analyzing the sensitivity to parameter spread we could indeed observe an improved stability over conventional RSFQ in all the cells that possess an internal state. We demonstrate the results for a toggle-flip-flop (TFF) with an ideal parameter set as shown in Fig. 5 [10].

The internal state of the π-shift TFF is represented by the circulating currents in the two flip-flop loops encompassing the storage inductance $L1$ (see Fig. 5). In the initial state, both π-rings carry the initial currents (marked with dashed arrows) corresponding to the π-phase shift in the loops. These currents favor the switching of $J2$ and $J3$ over $J4$ and $J5$ when a SFQ pulse enters the TFF through $J1$. Their switching toggles the

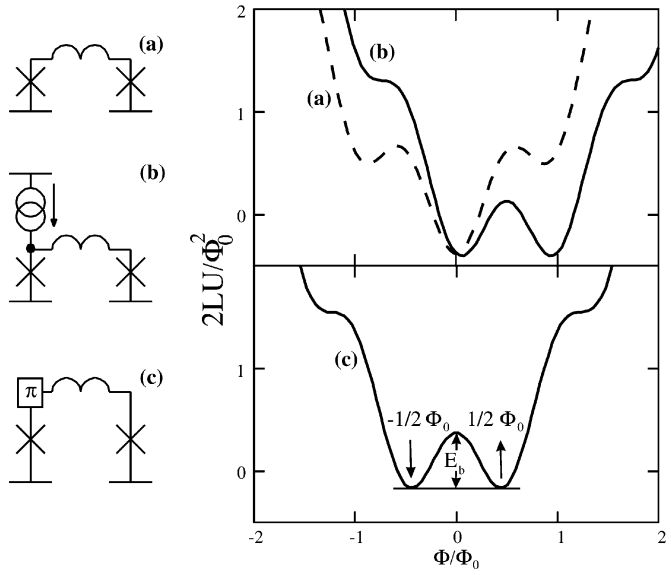

Fig. 4. Free energy U as a function of enclosed magnetic flux for three different superconducting loop configurations: (a) a standard two-junction SQUID loop; (b) a conventional RSFQ storage loop, comprising of a SQUID with an external current source; (c) the new configuration with an intrinsic π-phase shift.

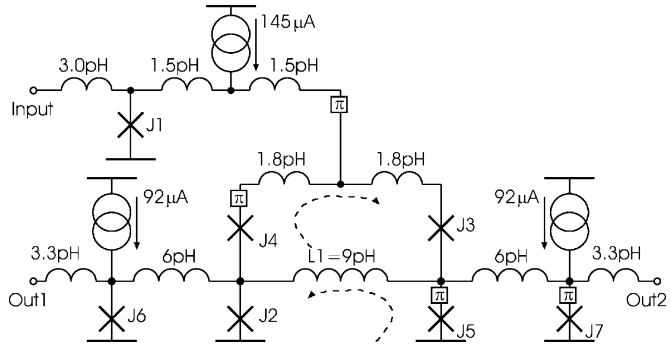

Fig. 5. Schematic of the TFF with two outputs. The critical currents of junctions $J1 \ldots J7$ are 126 μA.

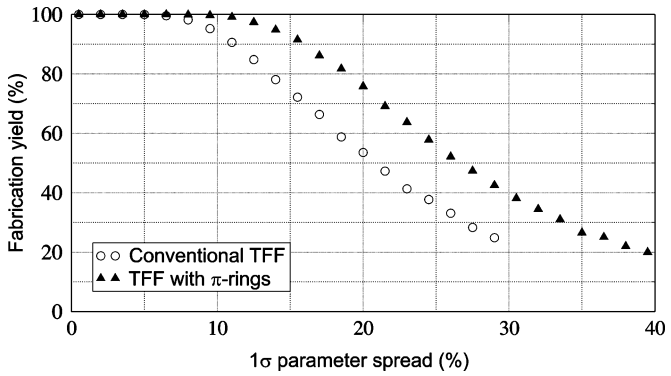

Fig. 6. Simulation of fabrication yield for our best conventional TFF in comparison to a realization including the features of π-rings. All critical currents, all bias currents and the global inductance scaling are normal distributed around the design value with the given standard deviation of σ.

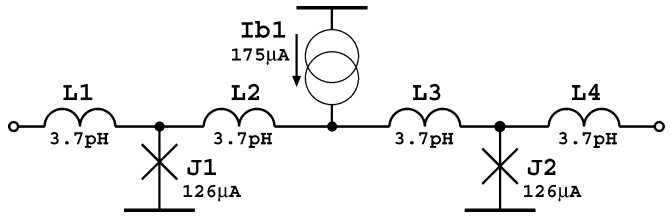

Fig. 7. Schematic and parameters for the Josephson transmission line as used in our first π-shift realization.

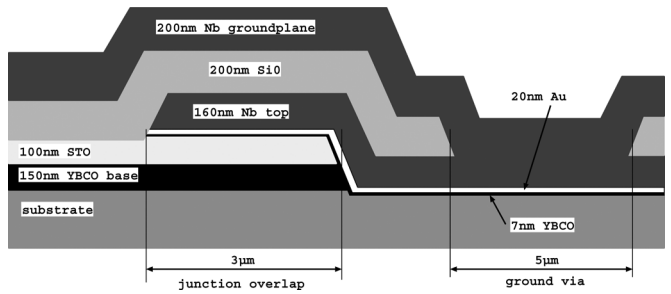

Fig. 8. Cross section of a ramp-type tunnel junction between YBCO and Nb with a gold barrier and an upper Nb-groundplane.

internal state, reversing the direction of the currents around the two loops, and an output pulse leaves the flip-flop through junction $J6$. If a second pulse arrives at the input it is transferred to the other output junction $J7$ by switching $J4$ and $J5$ this time, which toggles the internal state again to its initial position.

A Monte Carlo variation of all circuit parameters was performed to analyse the stability of the flip-flop against variations caused by the fabrication process. For that purpose, several thousand parameter-sets which had normal distributed random values with a standard deviation σ for all adjustable parameters (critical currents, inductances and bias currents) were used. The circuit's correct operation was checked by automatic circuit simulation runs. We used the parameters from the circuit realization containing π-rings [10] and the parameters for a standard Niobium 1 $\mathrm{kA/cm^2}$ realization of the FLUXONICS Foundry [11] for the simulation-based yield comparison shown in Fig. 6.

In RSFQ circuitry, SFQ pulses are usually fed to a flip-flop via a Josephson Transmission Line (JTL). Fig. 7 shows an example of this JTL circuit. Based on the layout of the JTL, cells are designed noticing the conditions for cell matching [12]. Standard library design methods are normally used, i.e., the bias level in different cells must be balanced so that only negligible currents will pass through their interfaces. Special care must also be taken to avoid creating additional loops with intrinsic π-phase shifts when interconnecting the cells. For instance, the two junctions in the JTL shown in Fig. 7 have to be π-junctions if the cells to which the JTL connects also have a π-junction at their interfaces. There is no significant advantage in using π-rings in a JTL, splitter, or confluence buffer, because these cells do not have an internal state and therefore the bistable mechanism of a loop with intrinsic π-phase shifts is dispensable.

IV. π-Shift RSFQ Circuit Realization and Experimental Results

The toggle-flip-flop with integrated π-loops was implemented using YBCO-Au-Nb ramp-type junction technology [13]. A cross-section of this type of junction is depicted in Fig. 8. The d-wave induced π-shifts have already been observed in SQUIDs containing these high-T_c to low-T_c Josephson junctions [14], and the spontaneous generation

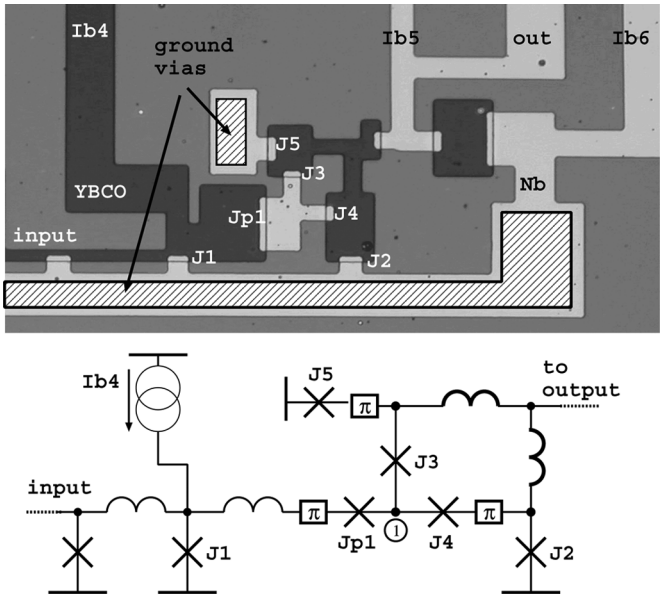

Fig. 9. The flip-flop kernel as the main part of the later shown final circuit (see right part of Fig. 12) is created by Josephson junctions $J2$–$J5$. The groundplane is not shown in this photograph, but the vias to ground are marked.

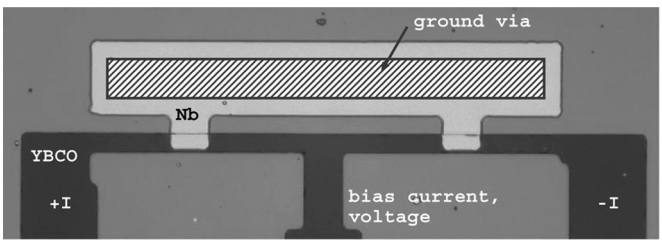

Fig. 10. Microphotograph of the SQUID structure before deposition of the top-groundplane.

of half-integer flux quanta related to these π-shifts has been demonstrated [15], [16]. Fig. 9 visualizes the actual toggle-flip flop, without any bias source in its core (usually connected to node 1). The junctions $J2$–$J5$ generate a total phase shift of π from node 1 to ground. To prevent a spontaneous circulating current, we need an extra π-shift between node 1 and the input driver junction $J1$. This π-shift is generated between $Jp1$ and $J1$. $Jp1$ is a non-switching (passive) junction behaving like a small parasitic inductor. The junction parameters were adjusted to obtain a critical current per junction width of 12 $\mu\mathrm{A}/\mu\mathrm{m}$. We estimated a maximum junction width of 13.5 $\mu\mathrm{m}$, above which we enter the long junction limit region, usually defined as four times the Josephson penetration depth.

RSFQ circuits require well defined inductances. Therefore, we modified the process by adding an upper Niobium groundplane to define microstrip lines and we calculated and measured inductance values for different configurations. The sheet inductances of YBCO and Nb and their temperature dependencies were measured using a SQUID structure as shown in Fig. 10. The measured inductance of Niobium microstrip lines fits well with calculations and reported values for standard Niobium processes. We measured higher inductance values of the YBCO-groundplane configuration in comparison to our assumptions.

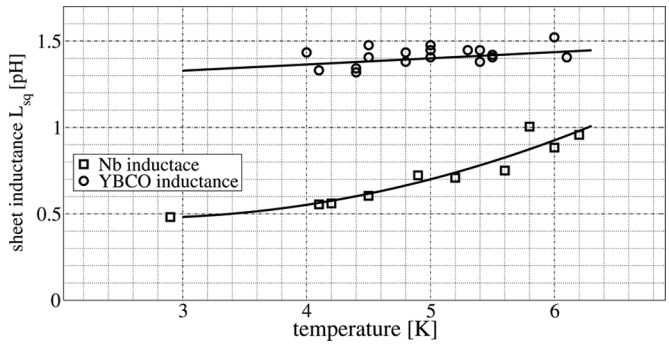

Fig. 11. Temperature dependence of the sheet inductance for a 5 $\mu\mathrm{m}$ wide microstrip line fabricated in YBCO as well as in Nb with respect to a Nb groundplane on top.

The plot in Fig. 11. gives a first impression of the sheet inductance values for the two mentioned layers. However, the numbers may change in further process development. The characteristic voltage of our first sample with groundplane is about 110 $\mu\mathrm{V}$, limiting the output voltage to 55 $\mu\mathrm{V}$. Previous single junction samples fabricated without groundplane show characteristic voltages up to 700 $\mu\mathrm{V}$, and it is our expectation that this will also be feasible with a groundplane.

To demonstrate the quantum precise operation, we create SFQ pulses in a classical dc/SFQ-converter and feed them via a JTL into the TFF. A micrograph of the sample after deposition of the groundplane and the complete circuit scheme with input and output circuitry is shown in Fig. 12. The TFF internal state can be read out with a two junction SQUID nested in the middle of the storage loop. The working point of the SQUID is adjusted by the bias currents $Ib5$ and $Ib6$ to create an output voltage for one state and no voltage for the other state. We measured the correct toggle-operation for each incoming SFQ pulse in the temperature range from 5.3 to 5.8 Kelvin at low speed. Fig. 13 shows the low speed measurement of the output voltage switching at each rising ramp of the input current. This is the first experimental proof for an RSFQ circuit operation based on the active switching of flux quanta between loops with an intrinsic π-phase shift.

In this sample, an extra ground plane layer was introduced for the first time to the standard fabrication process. This introduced a change in the nominal values of the current density of 30% and the YBCO sheet inductances of 100%. But even with this deviation from the design values, we could observe correct functioning in a range of $\pm 18\%$ for bias current $\mathrm{I}b4$, demonstrating the enhanced tolerance of our design. For future samples with critical current density and inductance values closer to the design values, we expect an operation range of $\pm 55\%$.

V. Conclusion

We have successfully demonstrated the digital operation of an RSFQ logic circuit with intrinsic π phase shifts, even with considerable parameter deviations between design and fabrication. This supports the predicted significant improvement in tolerance against parameter deviations by employing phase shifting elements in RSFQ electronics. Besides the advantage of strongly improved stability against parameter spread, circuits employing π-rings are more compact due to smaller inductances and less

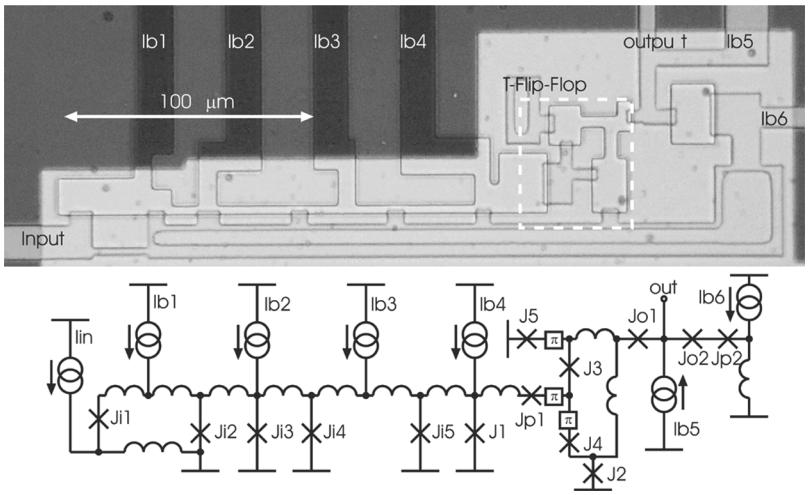

Fig. 12. Micrograph and schematic of the fabricated dc/SFQ-JTL-SFQ/dc circuit with the following junction widths: $J3, J4 : 7.5\ \mu\mathrm{m}$; $Jo1 : 8\ \mu\mathrm{m}$; $J1 : 9\ \mu\mathrm{m}$; $J2, Jo2 : 9.5\ \mu\mathrm{m}$; $Ji2 : 10\ \mu\mathrm{m}$; $Ji4, Ji5 : 10.5\ \mu\mathrm{m}$; $J5 : 11\ \mu\mathrm{m}$; $Ji1, Ji3 : 13\ \mu\mathrm{m}$. The two non-switching junctions $Jp1$, $Jp2$ are larger than the short junction limit. The critical current per unit width is $12\ \mu\mathrm{A}/\mu\mathrm{m}$.

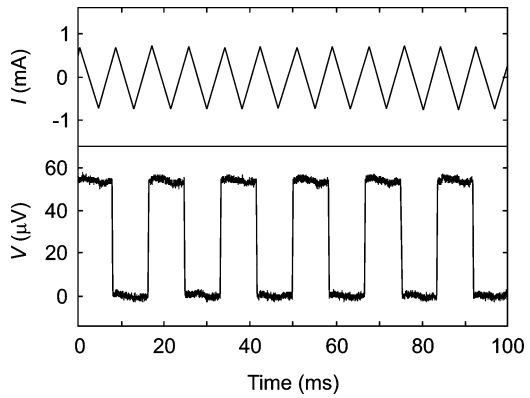

Fig. 13. The measured output voltage with a triangular input current of about 1 mA amplitude. On each rising ramp of this input signal a SFQ pulse is generated, then transferred to the TFF where it toggles its internal state. The output signal for a larger input signal is shown in [10].

bias current supplies. This leads to a simplification in the circuit design and smaller, more symmetric circuits with relaxed requirements to the fabrication process. Our first flip-flop realization needs only a quarter of the size of a standard TFF in established Niobium technology with the same feature size of about 2.5 $\mu\mathrm{m}$, even without having strived for miniaturization in this first design.

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